DATA SHEET

PCA9532
16-bit I^2C LED dimmer

Product data
Supersedes data of 2003 May 02

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Philips
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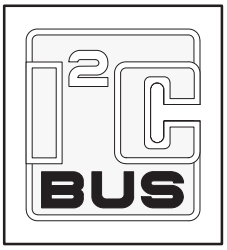
16-bit I²C LED dimmer PCA9532



FEATURES

- 16 LED drivers (on, off, flashing at a programmable rate)
- 2 selectable, fully programmable blink rates (frequency and duty cycle) between 0.591 and 152 Hz (1.69 seconds and 6.58 milliseconds)
- 256 brightness steps
- Input/outputs not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I²C-bus interface logic compatible with SMBus
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Active-LOW reset input
- 16 open drain outputs directly drive LEDs to 25 mA
- Controlled edge rates to minimize ground bounce
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO24, TSSOP24, HVQFN24

DESCRIPTION

The PCA9532 is a 16-bit I²C-bus and SMBus I/O expander optimized for dimming LEDs in 256 discrete steps for Red/Green/Blue (RGB) color mixing and back light applications.

The PCA9532 contains an internal oscillator with two user programmable blink rates and duty cycles coupled to the output PWM. The LED brightness is controlled by setting the blink rate high enough (> 100 Hz) that the blinking cannot be seen and then using the duty cycle to vary the amount of time the LED is on and thus the average current through the LED.

The initial set-up sequence programs the two blink rates/duty cycles for each individual PWM. From then on, only one command from the bus master is required to turn individual LEDs ON, OFF, BLINK RATE 1 or BLINK RATE 2. Based on the programmed frequency and duty cycle, BLINK RATE 1 and BLINK RATE 2 will cause the LEDs to appear at a different brightness or blink at periods up to 1.69 seconds. The open drain outputs directly drive the LEDs with maximum output sink current of 25 mA per bit and 200 mA per package (100 mA per octal).

To blink LEDs at periods greater than 1.69 seconds the bus master (MCU, MPU, DSP, chipset, etc.) must send repeated commands to turn the LED on and off as is currently done when using normal I/O Expanders like the Philips PCF8575 or PCA9555. Any bits not used for controlling the LEDs can be used for General Purpose Parallel Input/Output (GPIO) expansion which provides a simple solution when additional I/O is needed for ACPI power switches, sensors, pushbuttons, alarm monitoring, fans, etc.

The active-LOW hardware reset pin ($\overline{\text{RESET}}$) and Power-On Reset (POR) initializes the registers to their default state, all zeroes, causing the bits to be set HIGH (LED off).

Three hardware address pins on the PCA9532 allow eight devices to operate on the same bus.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
24-pin plastic SO	–40 °C to +85 °C	PCA9532D	PCA9532D	SOT137-1
24-pin plastic TSSOP	–40 °C to +85 °C	PCA9532PW	PCA9532	SOT355-1
24-pin plastic HVQFN	–40 °C to +85 °C	PCA9532BS	9532	SOT616-1

Standard packing quantities and other packaging data are available at www.standardproducts.philips.com/packaging.
I²C is a trademark of Philips Semiconductors Corporation.

PIN CONFIGURATION — SO, TSSOP

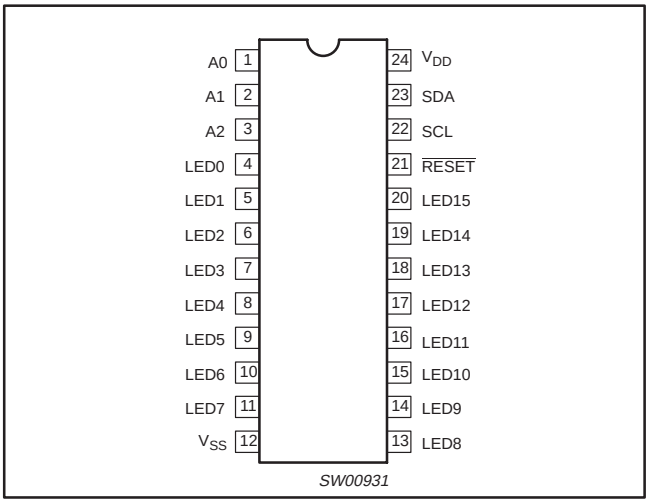


Figure 1. Pin configuration — SO, TSSOP

PIN CONFIGURATION — HVQFN

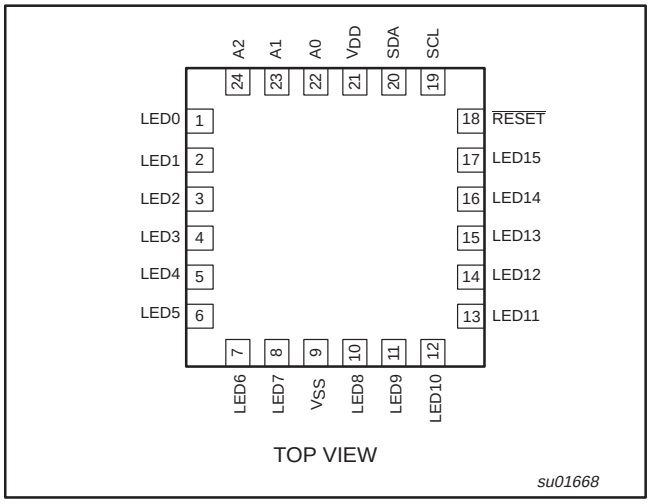


Figure 2. Pin configuration — HVQFN

PIN DESCRIPTION

PIN NUMBER		SYMBOL	FUNCTION
SO, TSSOP	HVQFN		
1	22	A0	Address input 0
2	23	A1	Address input 1
3	24	A2	Address input 2
4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8	LED0–7	LED driver 0–7
12	9	V_{SS}	Supply ground
13, 14, 15, 16, 17, 18, 19, 20	10, 11, 12, 13, 14, 15, 16, 17	LED8–15	LED driver 8–15
21	18	$\overline{RESET}$	Active-LOW reset input
22	19	SCL	Serial clock line
23	20	SDA	Serial data line
24	21	V_{DD}	Supply voltage

BLOCK DIAGRAM

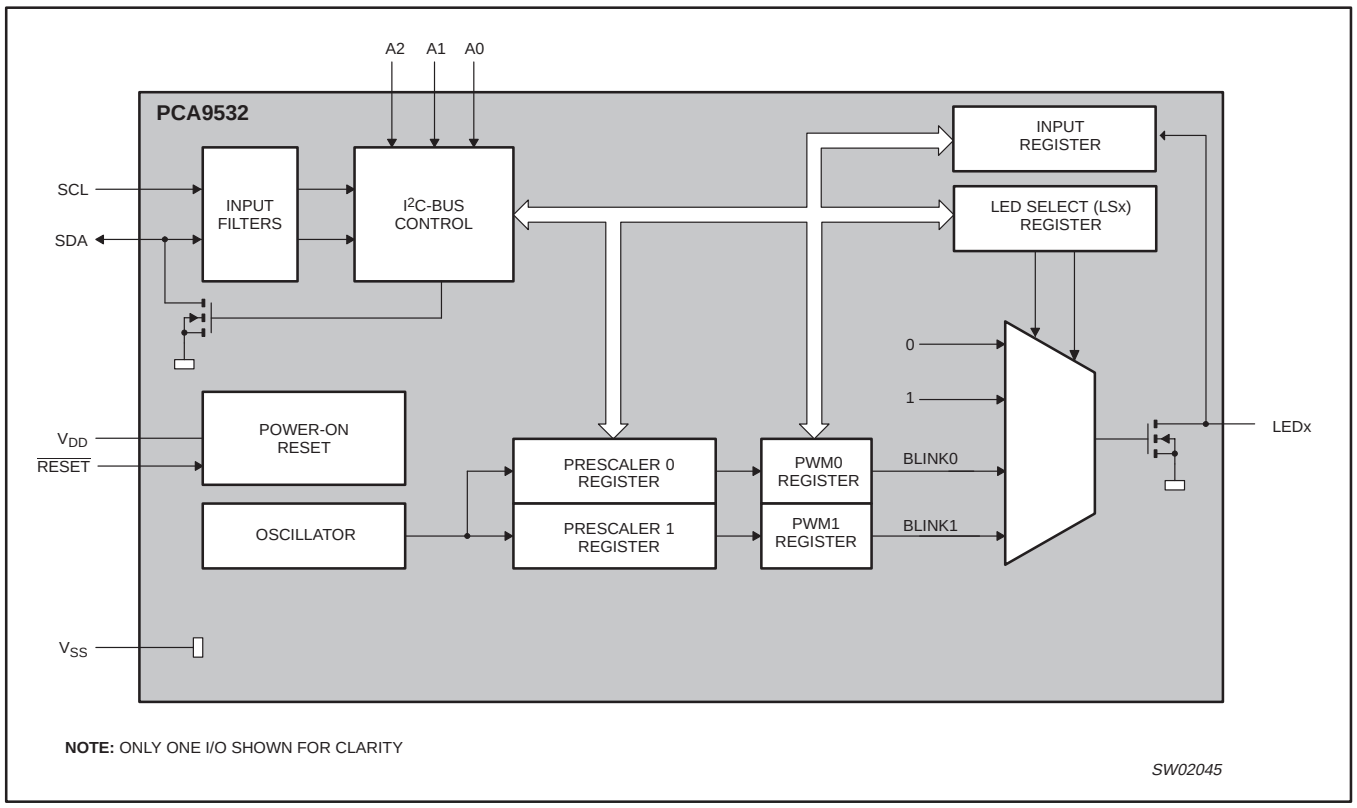


Figure 3. Block diagram

DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9532 is shown in Figure 4. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

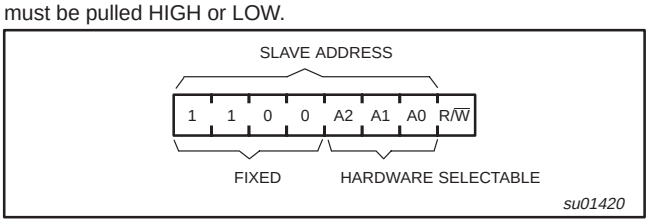


Figure 4. Slave address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected while a logic 0 selects a write operation.

CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9532 which will be stored in the Control Register. This register can be read and written via the I²C-bus.

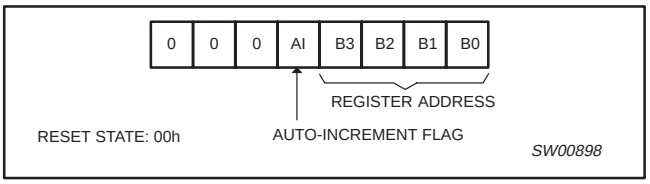


Figure 5. Control register

The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the auto-increment flag (AI) is set, the four low order bits of the Control Register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The contents of these bits will rollover to '0000' after the last register is accessed.

When auto-increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from '0' (B3 B2 B1 B0 ≠ 0 0 0 0)

Only the 4 least significant bits are affected by the AI flag.

Unused bits must be programmed with zeroes.

Control Register definition

B3	B2	B1	B0	REGISTER NAME	TYPE	REGISTER FUNCTION
0	0	0	0	INPUT0	READ	INPUT REGISTER 0
0	0	0	1	INPUT1	READ	INPUT REGISTER 1
0	0	1	0	PSC0	READ/ WRITE	FREQUENCY PRESCALER 0
0	0	1	1	PWM0	READ/ WRITE	PWM REGISTER 0
0	1	0	0	PSC1	READ/ WRITE	FREQUENCY PRESCALER 1
0	1	0	1	PWM1	READ/ WRITE	PWM REGISTER 1
0	1	1	0	LS0	READ/ WRITE	LED 0–3 SELECTOR
0	1	1	1	LS1	READ/ WRITE	LED 4–7 SELECTOR
1	0	0	0	LS2	READ/ WRITE	LED 8–11 SELECTOR
1	0	0	1	LS3	READ/ WRITE	LED 12–15 SELECTOR

REGISTER DESCRIPTION

INPUT0 — INPUT REGISTER 0

	LED 7	LED 6	LED 5	LED 4	LED 3	LED 2	LED 1	LED 0
bit	7	6	5	4	3	2	1	0
default	X	X	X	X	X	X	X	X

The INPUT register 0 reflects the state of the device pins (inputs 0 to 7). Writes to this register will be acknowledged but will have no effect.

NOTE: The default value "X" is determined by the externally applied logic level, normally '1' when used for directly driving LED with pull-up to V_{DD}.

INPUT1 — INPUT REGISTER 1

	LED 15	LED 14	LED 13	LED 12	LED 11	LED 10	LED 9	LED 8
bit	7	6	5	4	3	2	1	0
default	X	X	X	X	X	X	X	X

The INPUT register 1 reflects the state of the device pins (inputs 8 to 15). Writes to this register will be acknowledged but will have no effect.

NOTE: The default value "X" is determined by the externally applied logic level, normally '1' when used for directly driving LED with pull-up to V_{DD}.

PSC0 — FREQUENCY PRESCALER 0

bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

PSC0 is used to program the period of the PWM output.

$$\text{The period of BLINK0} = \frac{(\text{PSC0} + 1)}{152}$$

PWM0 — PWM REGISTER 0

bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

The PWM0 register determines the duty cycle of BLINK0. The outputs are LOW (LED on) when the count is less than the value in PWM0 and HIGH (LED off) when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always HIGH (LED off).

The duty cycle of BLINK0 is: $\frac{PWM0}{256}$

PSC1 — FREQUENCY PRESCALER 1

bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

PSC1 is used to program the period of PWM output.

The period of BLINK1 $= \frac{(PSC1 + 1)}{152}$

PWM1 — PWM REGISTER 1

bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED on) when the count is less than the value in PWM1 and HIGH (LED off) when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always HIGH (LED off).

The duty cycle of BLINK1 is: $\frac{PWM1}{256}$

LS0 — LED 0–3 SELECTOR

	LED 3		LED 2		LED 1		LED 0	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

LS1 — LED 4–7 SELECTOR

	LED 7		LED 6		LED 5		LED 4	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

LS2 — LED 8–11 SELECTOR

	LED 11		LED 10		LED 9		LED 8	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

LS3 — LED 12–15 SELECTOR

	LED 15		LED 14		LED 13		LED 12	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

The LSx LED select registers determine the source of the LED data.

00 = Output is set Hi-Z (LED off – default)
01 = Output is set LOW (LED on)
10 = Output blinks at PWM0 rate
11 = Output blinks at PWM1 rate

PINS USED AS GENERAL PURPOSE I/Os

LED pins not used to control LEDs can be used as general purpose I/Os.

For use as input: Set LEDx to high-impedance (00) and then read the pin state via the input register.

For use as output: Connect external pull-up resistor to the pin and size it according to the DC recommended operating characteristics. LED output pin is HIGH when the output is programmed as high-impedance, and LOW when the output is programmed LOW through the “LED selector” register. The output can be pulse-width controlled when PWM0 or PWM1 are used.

POWER-ON RESET

When power is applied to V_{DD}, an internal Power-On Reset holds the PCA9532 in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9532 registers are initialized to their default states, all the outputs in the off state. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

EXTERNAL RESET

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of t_W. The PCA9532 registers and I²C state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH.

This input requires a pull-up resistor to V_{DD} if no active connection is used.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 6).

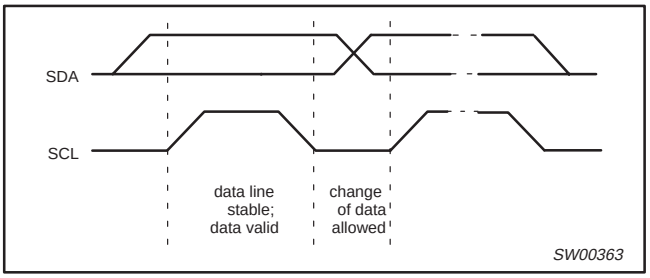


Figure 6. Bit transfer

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 7).

System configuration

A device generating a message is a transmitter: a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 8).

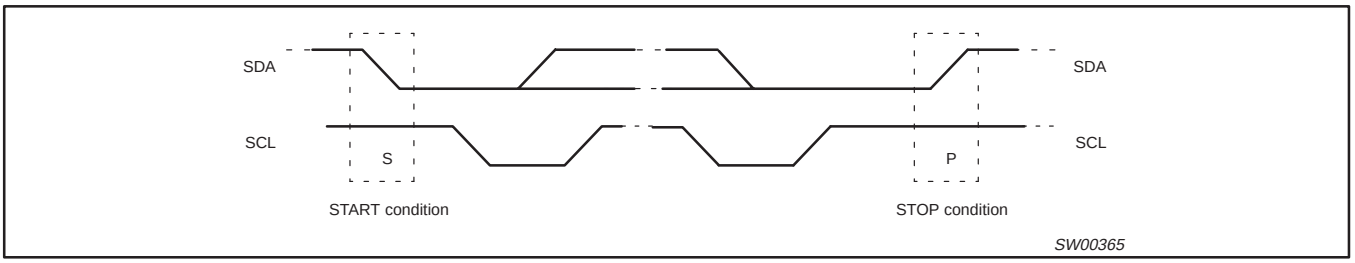


Figure 7. Definition of start and stop conditions

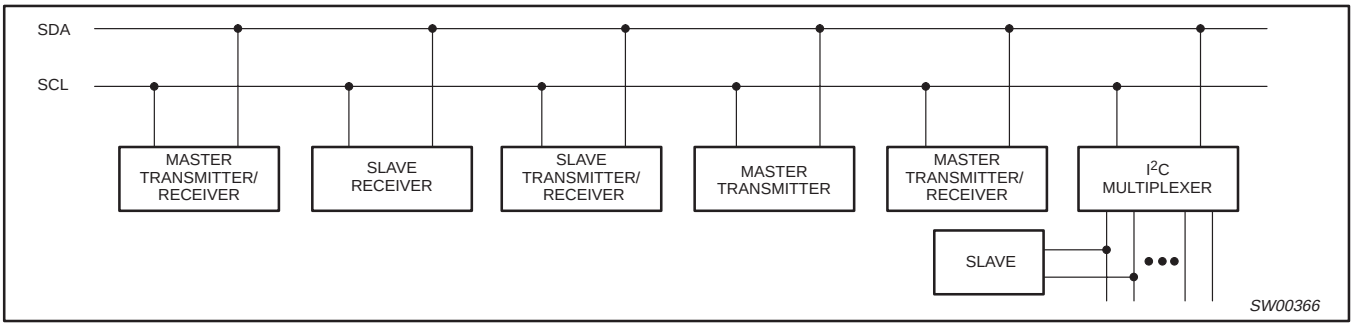


Figure 8. System configuration

Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH-level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

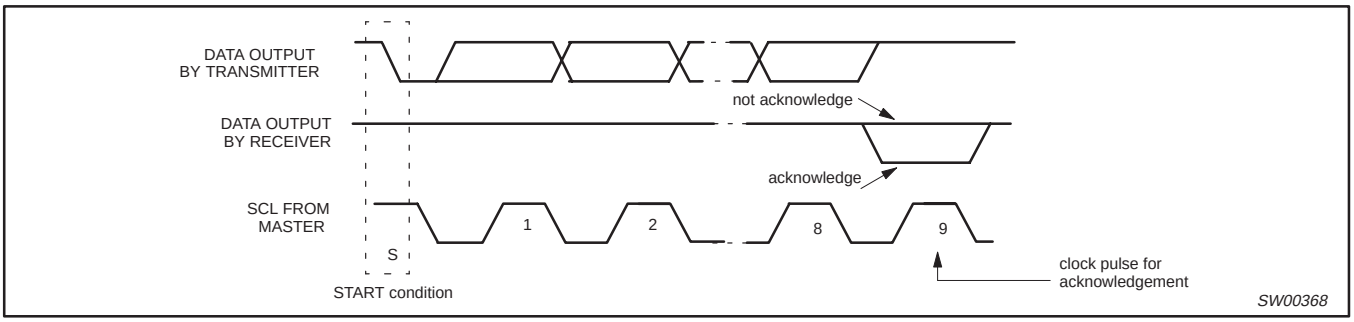


Figure 9. Acknowledgement on the I2C-bus

Bus transactions

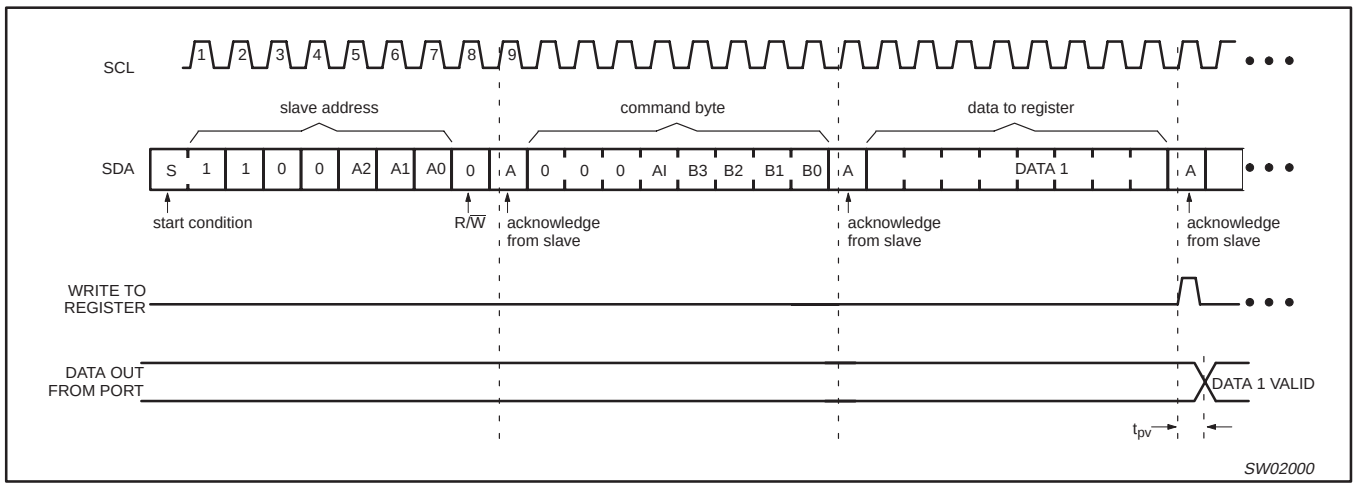


Figure 10. WRITE to register

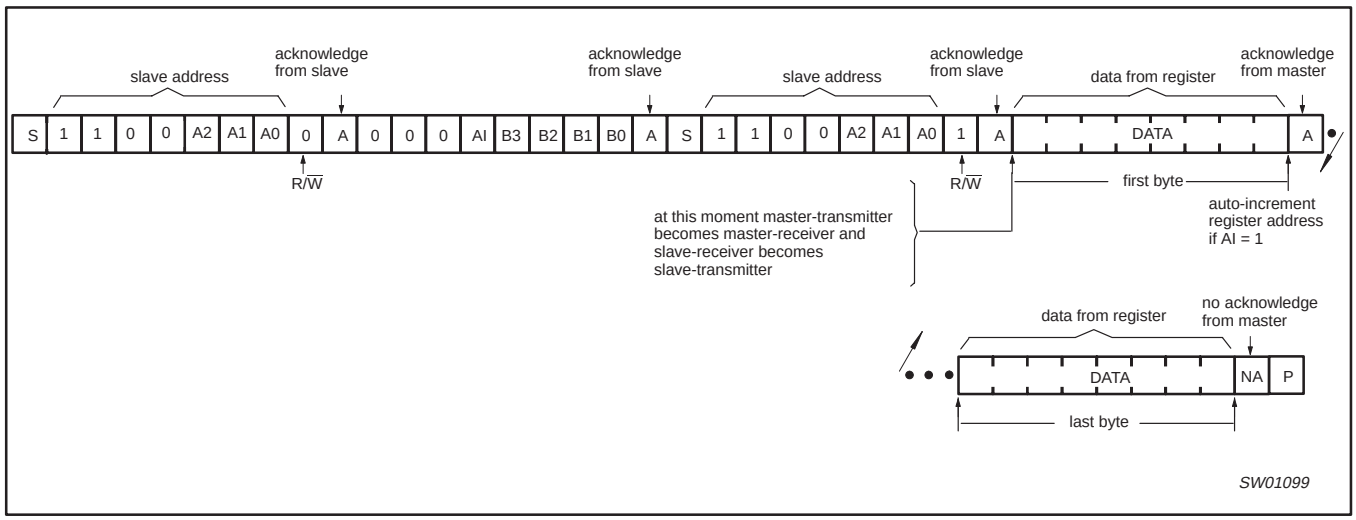
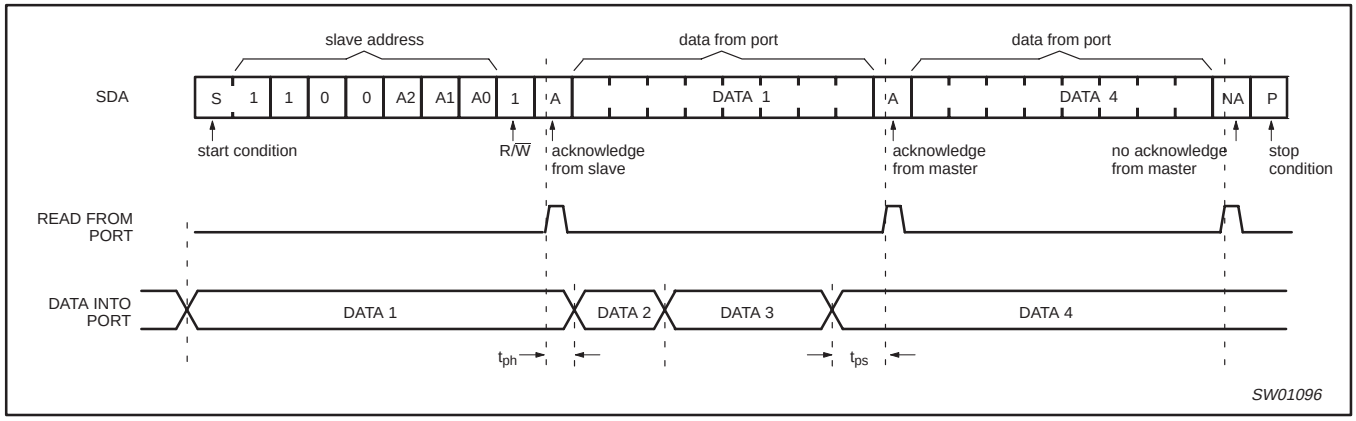


Figure 11. READ from register



NOTE:
1. This figure assumes the command byte has previously been programmed with 00h.

Figure 12. READ input port register

APPLICATION DATA

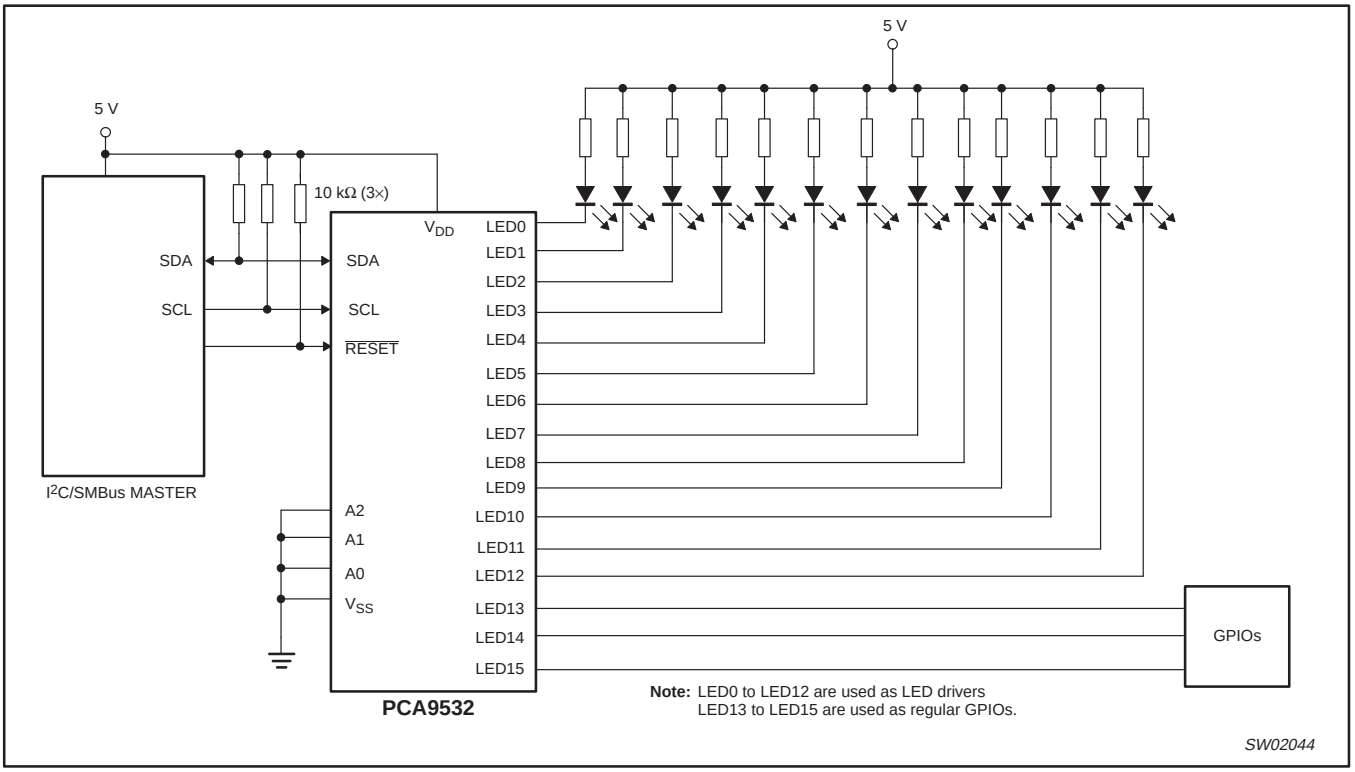


Figure 13. Typical application

Minimizing I_{DD} when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 13. Since the LED acts as a diode, when the LED is off the I/O V_{IN} is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_{IN} becomes lower than V_{DD} and is specified as ΔI_{DD} in the DC characteristics table.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 14 shows a high value resistor in parallel with the LED. Figure 15 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{DD} and prevents additional supply current consumption when the LED is off.

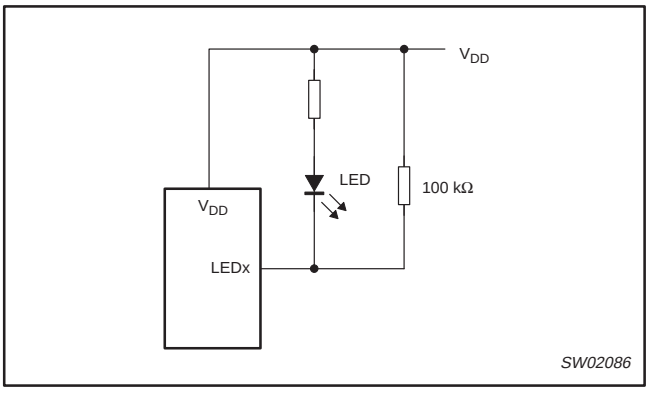


Figure 14. High value resistor in parallel with the LED

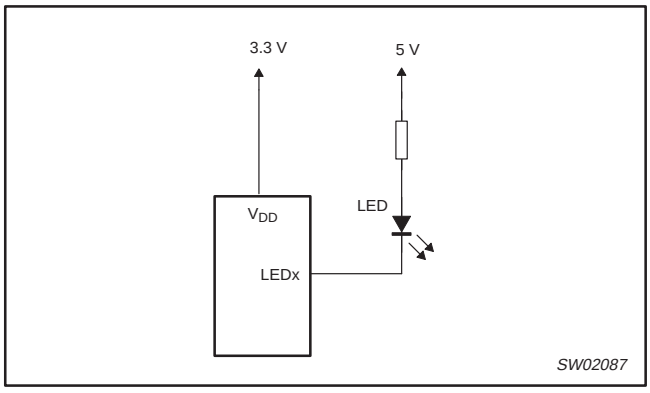


Figure 15. Device supplied by a lower voltage

Programming example

The following example will show how to set LED0 to LED3 on. It will then set LED4 and LED5 to blink at 1 Hz at a 50% duty cycle. LED6 and LED7 will be set to be dimmed at 25% of their brightness (duty cycle = 25%). LED8 to LED15 will be set to off.

Table 1.

	I²C-bus
Start	S
PCA9532 address with A0–A2 = LOW	C0h
PSC0 subaddress + auto-increment	12h
Set prescaler PSC0 to achieve a period of 1 second: $\text{Blink period} = 1 = \frac{\text{PSC0} + 1}{152}$ PSC0 = 151	97h
Set PWM0 duty cycle to 50%: $\frac{\text{PWM0}}{256} = 0.5$ PWM0 = 128	80h
Set prescaler PCS1 to dim at maximum frequency $\text{Blink period} = \text{maximum}$ PSC1 = 0	00h
Set PWM1 output duty cycle to 25%: $\frac{\text{PWM1}}{256} = 0.25$ PWM1 = 64	40h
Set LED0 to LED3 on	55h
Set LED4 and 5 to PWM0, and LED6 or 7 to PWM1	FAh
Set LED8 to LED11 off	00h
Set LED12 to LED15 off	00h
Stop	P

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	6.0	V
$V_{I/O}$	DC voltage on an I/O		V_{SS} – 0.5	5.5	V
$I_{I/O}$	DC output current on an I/O		—	±25	mA
I_{SS}	Supply current		—	200	mA
P_{tot}	Total power dissipation		—	400	mW
T_{stg}	Storage temperature range		–65	+150	°C
T_{amb}	Operating ambient temperature		–40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "*Handling MOS devices*".

DC CHARACTERISTICS

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified. TYP at 3.3 V and 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Supply voltage		2.3	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 100 kHz	—	350	550	µA
I_{stb}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 0 kHz	—	2.1	5.0	µA
ΔI_{DD}	Additional standby current	Standby mode; V_{DD} = 5.5 V; Every LED I/O at V_{IN} = 4.3 V; f_{SCL} = 0 kHz	—	—	2	mA
V_{POR}	Power-on reset voltage (Note 1)	V_{DD} = 3.3 V; no load; $V_I = V_{DD}$ or V_{SS}	—	1.7	2.2	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		–0.5	—	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	6.5	—	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	–1	—	+1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	4.4	5	pF
I/Os						
V_{IL}	LOW-level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2.0	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V; Note 2	9	—	—	mA
		V_{OL} = 0.4 V; V_{DD} = 3.0 V; Note 2	12	—	—	mA
		V_{OL} = 0.4 V; V_{DD} = 5.0 V; Note 2	15	—	—	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V; Note 2	15	—	—	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V; Note 2	20	—	—	mA
		V_{OL} = 0.7 V; V_{DD} = 5.0 V; Note 2	25	—	—	mA
I_L	Input leakage current	V_{DD} = 3.6 V; V_I = 0 V or V_{DD}	–1	—	1	µA
C_{IO}	Input/output capacitance		—	2.6	5	pF
Select Inputs A0, A1, A2 / $\overline{\text{RESET}}$						
V_{IL}	LOW-level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2.0	—	5.5	V
I_{LI}	Input leakage current		–1	—	1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	2.3	5	pF

NOTE:

1. V_{DD} must be lowered to 0.2 V in order to reset part.
2. Each I/O must be externally limited to a maximum of 25 mA and each octal (LED0–LED7 and LED8–LED15) must be limited to a maximum current of 100 mA for a device total of 200 mA.

AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I²C-BUS		FAST MODE I²C-BUS		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	µs
$t_{SU;STA}$	Repeated START condition set-up time	4.7	—	0.6	—	µs
$t_{SU;STO}$	Setup time for STOP condition	4.0	—	0.6	—	µs
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;ACK}$	Valid time for ACK condition[2]	—	600	—	600	ns
$t_{VD;DAT}$ (L)	Data out valid time[3]	—	600	—	600	ns
$t_{VD;DAT}$ (H)	Data out valid time[3]	—	1500	—	600	ns
$t_{SU;DAT}$	Data set-up time	250	—	100	—	ns
t_{LOW}	Clock LOW period	4.7	—	1.3	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	0.6	—	µs
t_F	Clock/Data fall time	—	300	20 + 0.1 C_b[1]	300	ns
t_R	Clock/Data rise time	—	1000	20 + 0.1 C_b[1]	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
Port Timing						
t_{PV}	Output data valid	—	200	—	200	ns
t_{PS}	Input data set-up time	100	—	100	—	ns
t_{PH}	Input data hold time	1	—	1	—	µs
Reset						
t_W	Reset pulse width	10	—	10	—	ns
t_{REC}	Reset recovery time	0	—	0	—	ns
t_{RESET}[4,5]	Time to reset	400	—	400	—	ns

NOTES:
1. C_b = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
4. Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.
5. Upon reset, the full delay will be the sum of t_{RESET} and the RC time constant of the SDA bus.

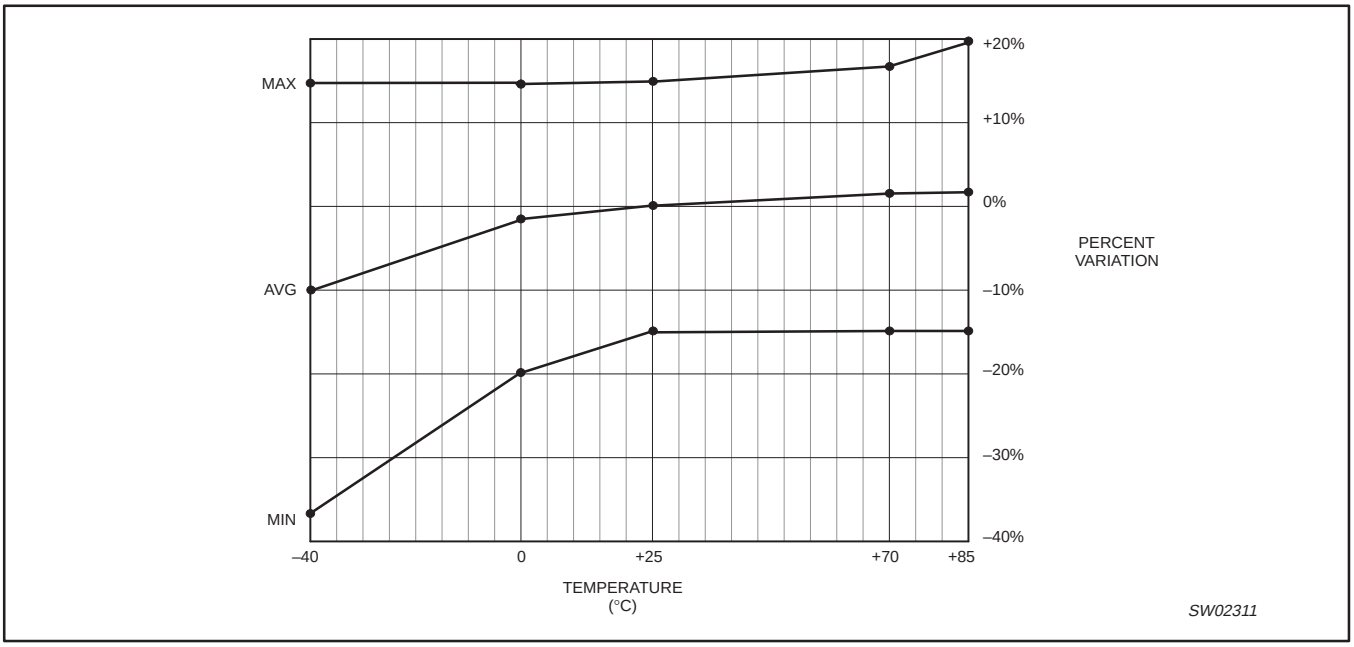


Figure 16. Typical frequency variation over process at V_{DD} = 2.3 V to 3.0 V

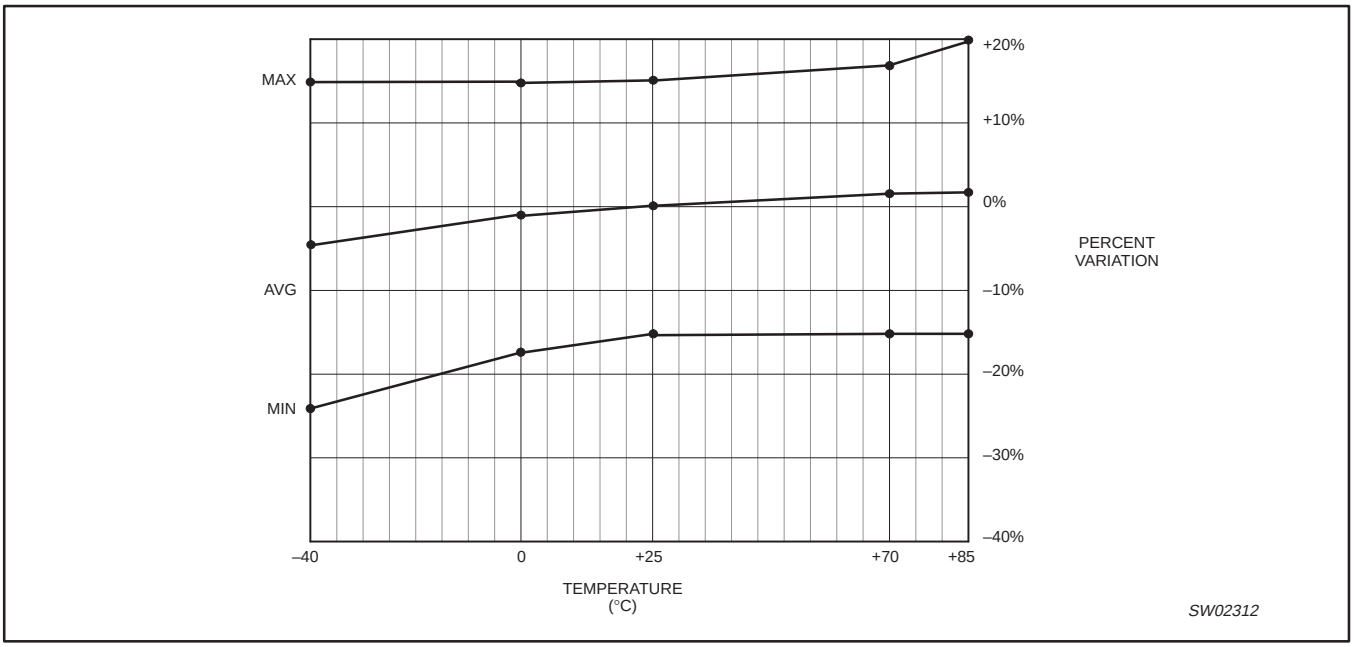


Figure 17. Typical frequency variation over process at V_{DD} = 3.0 V to 5.5 V

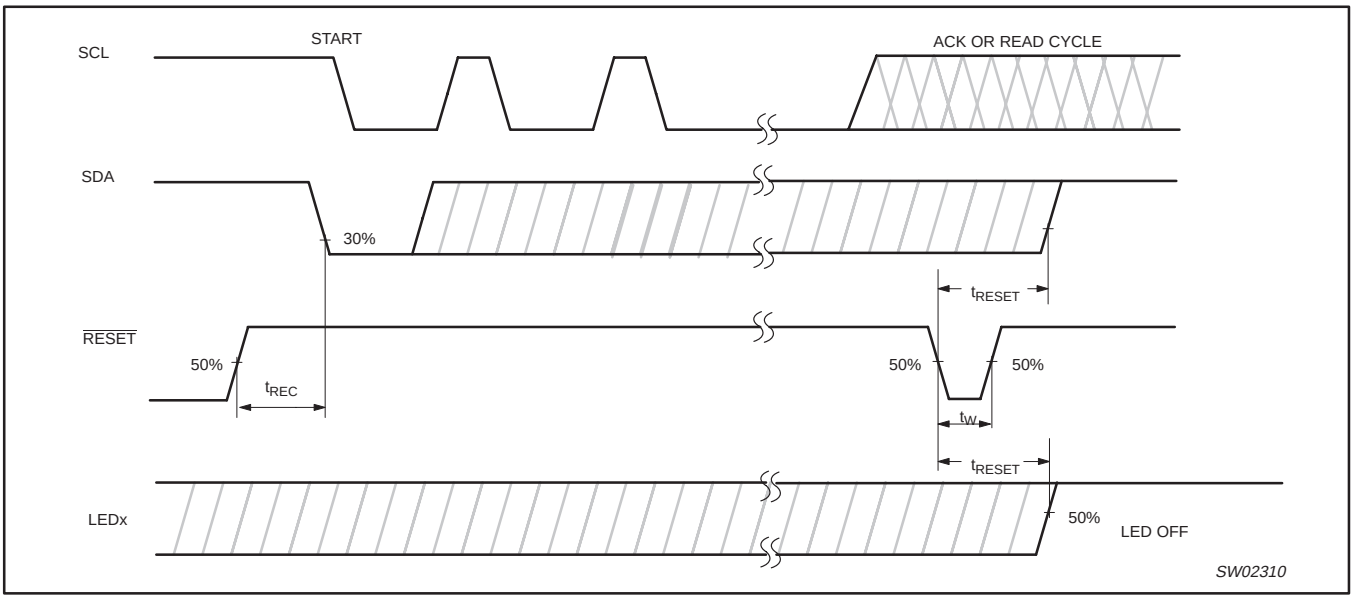


Figure 18. Definition of $\overline{\text{RESET}}$ timing

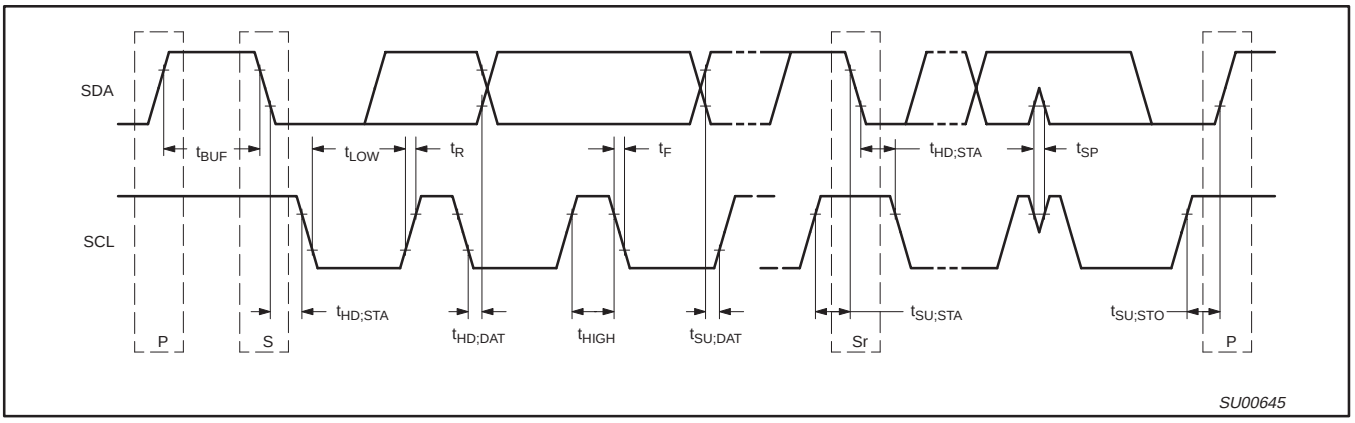


Figure 19. Definition of timing

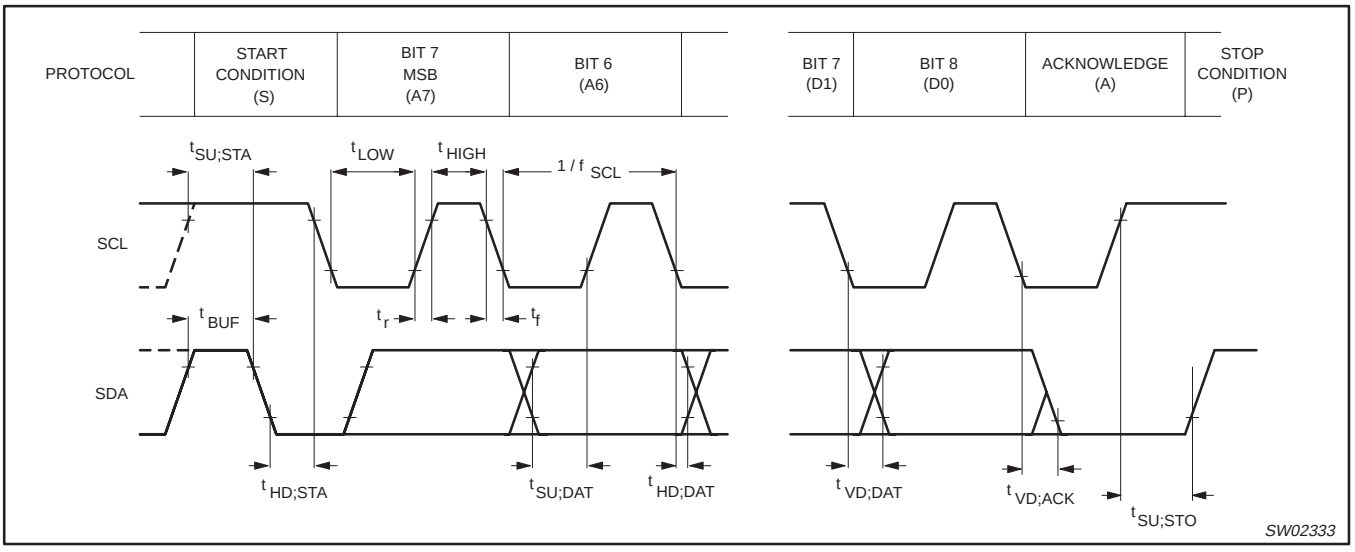
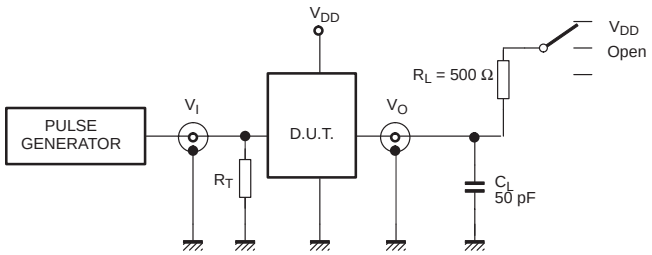


Figure 20. I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}



DEFINITIONS

R_L = Load resistor FOR LEDN. R_L FOR SDA AND SCL > 1 kΩ (3 mA or less current).

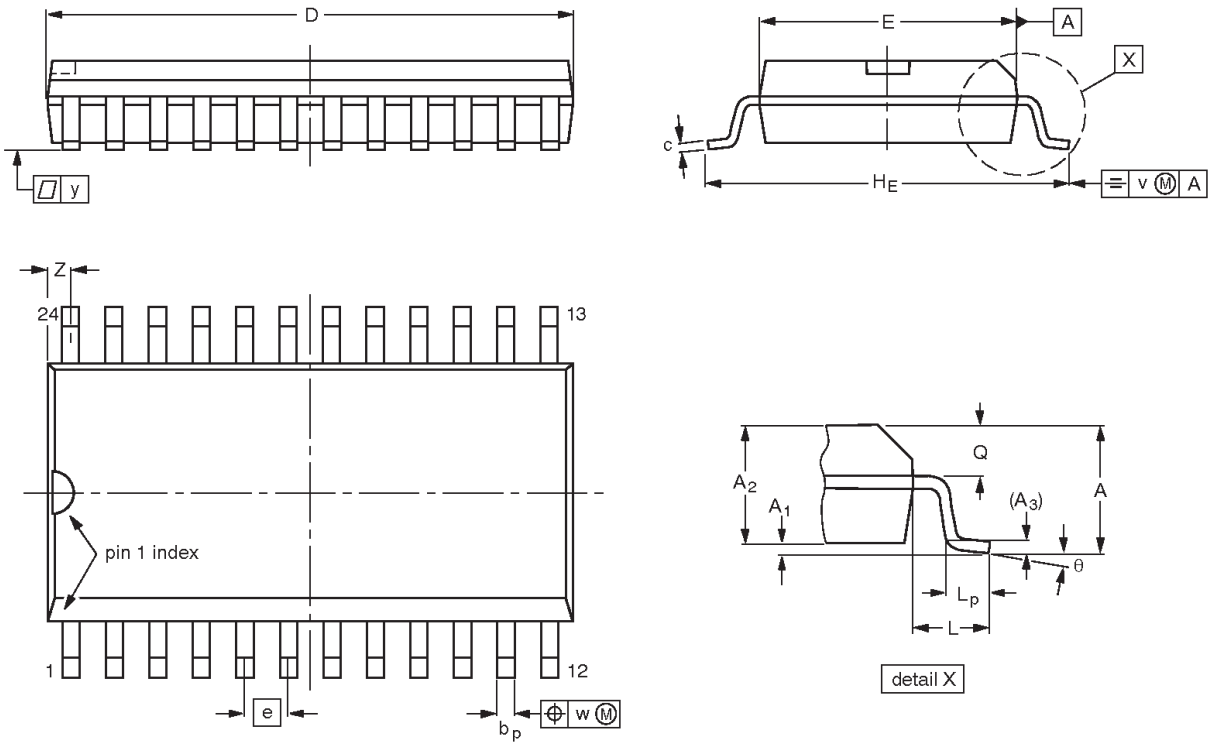
C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generators.

SW02334

Figure 21. Test circuitry for switching times

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

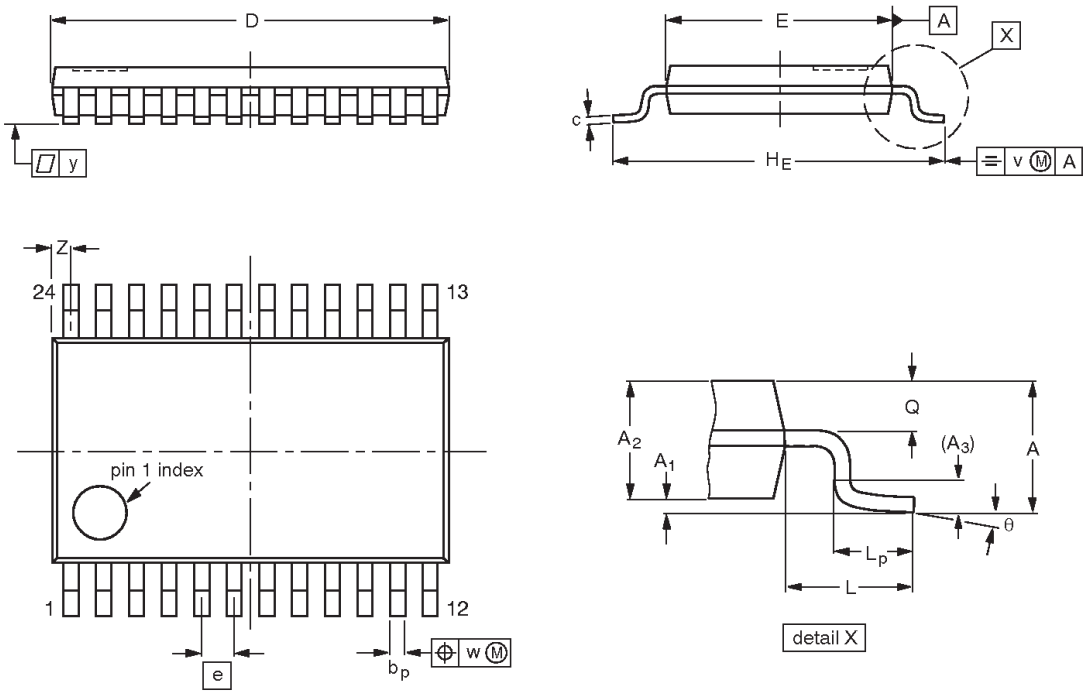
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

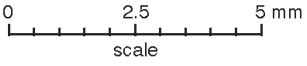
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**





DIMENSIONS (mm are the original dimensions)

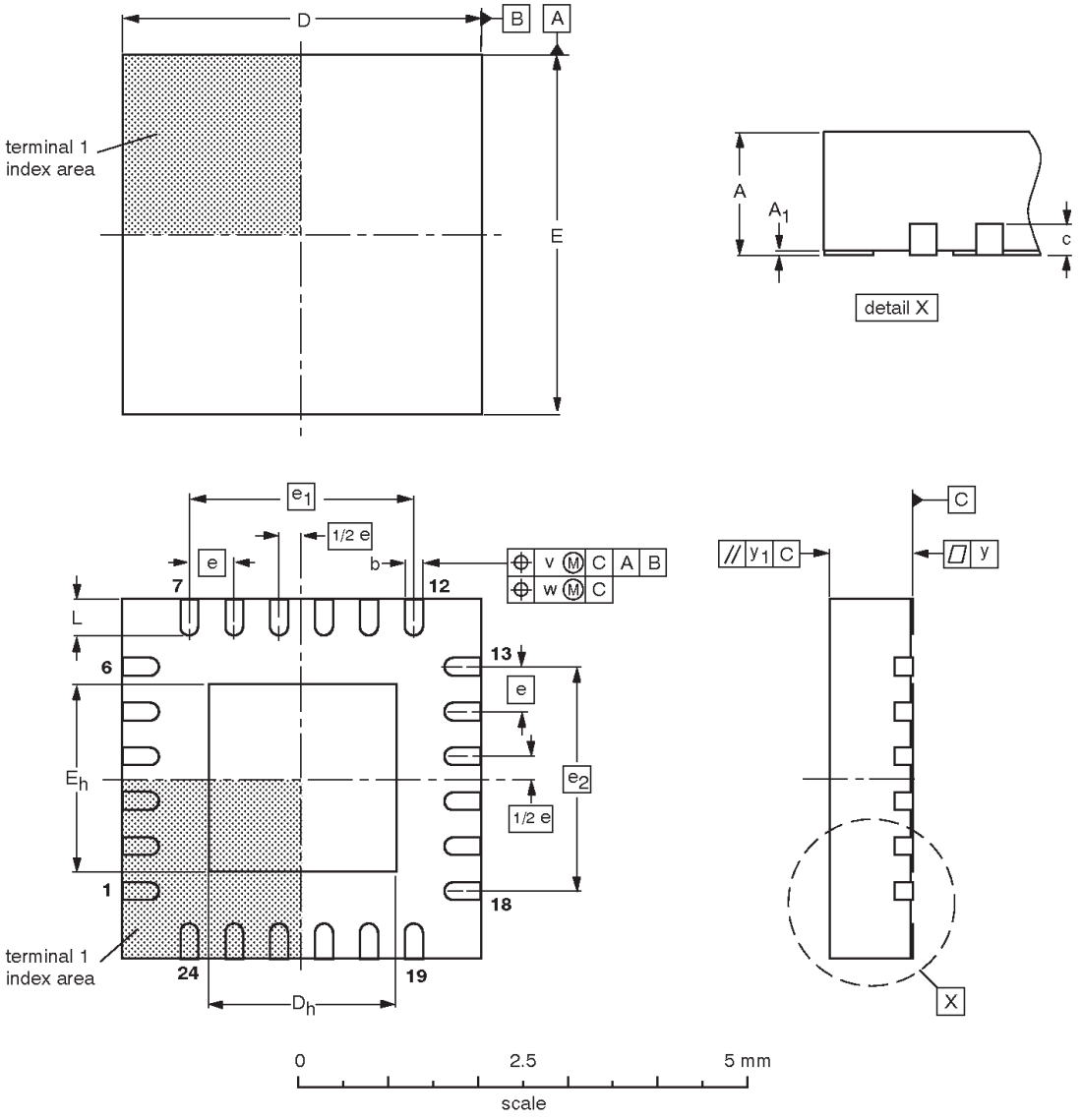
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

REVISION HISTORY

Rev	Date	Description
_3	20041001	**Product data sheet (9397 750 13691); Supersedes data of 02 May 2003 (9397 750 11459).** Modifications: ● "Features" section on page 2: – second bullet: change from "... between 0.625 and 160 Hz (6.4 seconds and 6.25 milliseconds)" to "... between 0.591 Hz and 152 Hz (1.69 seconds and 6.58 milliseconds)" ● "Description" section on page 2: – Third paragraph, third sentence: change from "... or blink at periods up to 1.6 second." to "... or blink at periods up to 1.69 second." – Fourth paragraph, first sentence: change from "... periods greater than 1.6 seconds ..." to "... periods greater than 1.69 seconds." ● Page 5: – from "INPUT0 — INPUT REGISTER 1" to "INPUT0 — INPUT REGISTER 0"; and in the paragraph following the table: from "The INPUT register 1 reflects ..." to "The INPUT register 0 reflects ..." – from "INPUT1 — INPUT REGISTER 2" to "INPUT1 — INPUT REGISTER 1" ● Section "INPUT0 — INPUT REGISTER 0" on page 5 – add note – table re-written ● Section "INPUT1 — INPUT REGISTER 1" on page 5 – add note – table re-written ● Add section "Pins used as General Purpose I/Os" on page 6. ● Section "Power-on reset" on page 6 re-written. ● Section "External reset" on page 6: second paragraph re-written. ● Figure 13 on page 10: add resistor values. ● (New) Note 1 added to DC Characteristics table on page 12, and its reference added at parameter V_{POR}. ● Figure 18 modified. ● Added Figures 20 and 21.
_2	20030502	**Product data (9397 750 11459); ECN 853-2398 29860 dated 24 April 2003. Supersedes data of 26 February 2003 (9397 750 10874).**
_1	20030226	Product data (9397 750 10874); ECN 853–2398 29297 of 12 December 2002.

16-bit I²C LED dimmer PCA9532

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